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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,068	12/29/2003	Oceager P. Yee	Yee 7	8296

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EXAMINER	
LIN, SUN J	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/748,068	YEE, OCEAGER P.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/29/03,06/16/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/748,068 filed on 012/29/2003. Claims 1 – 20 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim1, line 2, change "said blocks" to **—said functional blocks—**.
Claim 1, line 3, before "steps" delete **—the—**.
Claim 1, line 6, before "occurrence" delete **—the—**.
Claim 3, line 1, before "step" delete **—the—**.
Claim 3, line 2, change "the internal" to **—an internal—**.
Claim 4, line 1, change "said blocks" to **—said functional blocks—**.
Claim 4, line 2, before "steps" delete **—the—**.
Claim 4, line 5, change "registers" to **—register element—**.
Claim 4, line 7, change "provide control of the selected scan chain to a scan clock signal" to **—provide a scan clock signal to control the selected scan chain—**.
Claim 5, line 1, before "steps" delete **—the—**.
Claim 5, line 2, change "environment" to **—components—**.
Claim 6, line 1, before "steps" delete **—the—**.
Claim 7, line 1, before "steps" delete **—the—**.
Claim 8, line 2, change "said blocks" to **—said functional blocks—**.
Claim 8, line 2, before "steps" delete **—the—**.
Claim 8, line 5, change "elements" to **—element—**.
Claim 9, line 1, before "steps" delete **—the—**.
Claim 9, line 4, before "occurrence" delete **—the—**.
Claim 10, line 1, before "steps" delete **—the—**.
Claim 10, line 2, change "one block" to **—one of said functional blocks—**.
Claim11, line 2, change "said blocks" to **—said functional blocks—**.
Claim 11, line 7, before " presence" delete **—the—**.
Claim 14, line 1, change "said blocks" to **—said functional blocks—**.
Claim 15, line 2, change "environment" to **—components—**.

Claim18, line 1, change "said blocks" to —**said functional blocks**—.
Claim 18, line 5, change "elements" to —**element**—.
Claim 20, line 2, change "one block" to —**one of said functional blocks**—.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,812,562 to *Baeg* in view of U.S. Patent No. 5,675,729 to *Mehring*.

5. As to Claim 1, *Baeg* shows and discloses the following subject matter:

- A method of using boundary scan chain and JTAG test port to facilitate *debugging integrated circuit chips* (i.e., *system-on-chip SOC*) mounted on a board – [col. 1, line 23 – 55; Fig. 2]; Notice that each *integrated circuit chip* is a system component include at least one a function block, each functional block is designed to provide a specific function required in the SOC;
- A functional block 203 is control by a block clock controlled by a *clock control unit 205* – [Fig. 2; abstract];
- Debugging steps apply *handshaking sequence* to ensure functional blocks under test are in a *known state* (i.e., *specific known event*) before the

associated clocks are *stopped* (i.e., *halted*) – [col. 4, line 32 – 58]; Observation Control Register (OCR) is used to observe (i.e., *monitor*) *internal states* (i.e., *events*) of the functional blocks – [col. 4, line 3 – 7];

- Breakpoints, instruction stepping – [col. 4, line 27].

Baeg does not clearly disclose a method of setting a breakpoint on a specific event occurring in a functional block on the SOC. But *Mehring* teach subject matter regarding this method as listed below:

- Generating a *breakpoint signal* (debug trigger signal) based on a number of counts of a specified event associated with performance information (i.e., state) of a functional block under study – [col. 3, line 1 – 15];
- Breakpoint trigger logic – [col. 4, line 66 – col. 5, line 1 – 11].
- Monitor events 410 – [Fi9. 6]; A hardware counters perform the task of *detecting* (i.e., *monitoring*) counts of events – [col. 3, line 4 – 7]; *Occurrence* of an event or events – [col. 3, line 13] Notice that each count number is associated with one event;
- Monitor events to generate breakpoint signal – [col. 4, line 39 – 40]; Breakpoint signal causes (i.e., triggers) clock controller to stop the clock such that an internal state of a scan register can be determined – [col. 3, line 36 – 40].

Notice that the hardware counters can be utilized to accurately monitor events occurring on each integrated circuit chips included in a SOC thereby correctly recognizing occurrence of a specific event for timely setting a breakpoint for generating a *breakpoint signal* (i.e., debug trigger signal) for use in debugging the SOC.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Mehring* in utilizing hardware counters in accurately monitoring events occurring on each integrated circuit chips included in a SOC thereby correctly recognizing occurrence of a specific event for timely setting a breakpoint for generating a breakpoint signal (debug trigger signal) for use in debugging the SOC.

It is well known in the art that states of system components can be examined by checking contents of JTAG scan registers, and the states can be utilized to debug the SOC.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

6. As to Claim 11, reasons are included in **[Response A]** given above.

7. As to Claims 2 and 12, *Mehring* teach that a process periodically read the state of counters to monitor counts of *specific event* – [col. 3, line 1 – 7]. Notice that the specific event is a "read instruction".

8. As to Claims 3 and 13, *Mehring* teaches the following subject matter:

- A breakpoint signal is generated (and sent) to clock controller of component (under study) which then stops the clock and *enables* the user to run an internal debug scan … to determine the *state* of the component – [col. 3, line 31 – 40];
- Generating an *output signal indicative* of a certain *state* of component (can be observed) – [col. 4, line 25 – 38].

9. As to Claims 4 and 14, *Baeg* shows and teaches the subject – [col. 4, line 32 – col. 5, line 40; Fig. 2; Fig. 6].

For reference purposes, the explanations given above in response to Claims 4 and 14 are called **[Response B]** hereinafter.

10. As to Claims 5 and 15, *Mehring* teaches the subject matter – [col. 3, line 23 – 29]. Notice that (1) reloading is an action of restoring (2) a "debug clear signal" is recognized when a "trigger signal" is not received.

11. As to Claims 6, 7, 16 and 17, in addition to reasons included in **[Response A]** given above, *Baeg* shows and teaches the following subject matter:

- Scan internal registers, it is necessary to stop system clocks going to the registers desired to be scanned ... selectively stop the clocks depending on how the values are set up in the MCR (*mode control register*) – [col. 5, line 22 – 27];
- TCK provides scan clocks for internal scan chains – [Fig. 2]; scan chain includes a number of *shift register latches* – [col. 6, 31 – 32];
- MCR controls clock control logic 205 and internal function blocks – [col. 3, line 63 – 64]; Observation Control Register (OCR) is used to observe (i.e., *monitor*) *internal states* (i.e., *events*) of the functional blocks – [col. 4, line 3 – 7].

According to JTAG scan standard, after performing an *single step execution* (i.e., single shifting) or *n-cycle step execution* (i.e., n-shifting) contents (i.e., states) of *internal scan shift register latches* included in a system component under study should be redetermined and/or updated.

For reference purposes, the explanations given above in response to Claims 6, 7, 16 and 17 are called **[Response C]** hereinafter.

12. As to Claims 8 and 18, reasons are included in **[Response A]**, **[Response B]** and **[Response C]** given above.

13. As to Claims 9 and 19, in addition to reasons included in **[Response A]** given above, *Mehring* teaches the following subject matter:

- Monitoring events to generate a breakpoint signal (debug trigger signal) – [col. 4, line 39 – 40];
- Breakpoint signal is generated due to occurrence of events (i.e., more than one specific event) – [col. 3, line 8 – 16].

14. As to Claims 10 and 20, reasons are included in **[Response C]** given above. Notice that the JTAG scan can be performed on a specific functional block by stopping it block clock and then performing an n-cycle step execution.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent examiner
Art Unit 2825
October 11, 2005